LEGAL NOTICE:

This NVM Express Management Interface revision 1.0a technical proposal is proprietary to the NVM Express, Inc. (also referred to as "Company") and/or its successors and assigns.

NOTICE TO USERS WHO ARE NVM EXPRESS, INC. MEMBERS: Members of NVM Express, Inc. have the right to use and implement this NVM Express Management Interface revision 1.0a technical proposal subject, however, to the Member's continued compliance with the Company's Intellectual Property Policy and Bylaws and the Member's Participation Agreement.

NOTICE TO NON-MEMBERS OF NVM EXPRESS, INC.: If you are not a Member of NVM Express, Inc. and you have obtained a copy of this document, you only have a right to review this document or make reference to or cite this document. Any such references or citations to this document must acknowledge NVM Express, Inc. copyright ownership of this document. The proper copyright citation or reference is as follows: **"© 2007 - 2018 NVM Express, Inc. ALL RIGHTS RESERVED."** When making any such citations or references to this document you are not permitted to revise, alter, modify, make any derivatives of, or otherwise amend the referenced portion of this document in any way without the prior express written permission of NVM Express, Inc. Nothing contained in this document shall be deemed as granting you any kind of license to implement or use this document or the specification described therein, or any of its contents, either expressly or impliedly, or to any intellectual property owned or controlled by NVM Express, Inc., including, without limitation, any trademarks of NVM Express, Inc.

LEGAL DISCLAIMER:

THIS DOCUMENT AND THE INFORMATION CONTAINED HEREIN IS PROVIDED ON AN "**AS IS**" BASIS. TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, NVM EXPRESS, INC. (ALONG WITH THE CONTRIBUTORS TO THIS DOCUMENT) HEREBY DISCLAIM ALL REPRESENTATIONS, WARRANTIES AND/OR COVENANTS, EITHER EXPRESS OR IMPLIED, STATUTORY OR AT COMMON LAW, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, VALIDITY, AND/OR NONINFRINGEMENT.

All product names, trademarks, registered trademarks, and/or servicemarks may be claimed as the property of their respective owners.

NVM Express Management Interface Workgroup
c/o NVM Express Administration
3855 SW 153rd Drive
Beaverton, OR 97003
admin@nvmexpress.org

NVM Express Technical Proposal for New Feature

Technical Proposal ID	**6004 – VPD Write Cycle Reduction**
Change Date	**1/28/2018**
Builds on Specification	**NVM Express Management Interface 1.0a**

Technical Proposal Author(s)

Name	Company
Frank Chu, Chris Sneed	WDC
Peter Onufryk	Microsemi
Austin Bolen	Dell EMC
Michael Allison	SKHMS
Myron Loewen	Intel

Description Goes Here:

1. Reducing the required write cycles from 100 down to 8 better enables use of OTP (e.g. eFuse) technology to integrate VPD as part of a device controller ASIC.

Revision History

Revision Date	Change Description
06/23/17	Initial draft.
07/24/17	Updates after NVMe-MI discussions on 7/24/17: a.. Adding a status bit to indicate no VPD write operation only under Vaux supply b. Adding a method for indicating how many remaining VPD cycles left c, Adding a status bit to indicate the count is a valid entry
07/25/17	This is TP 004
08/18/17	Editorial updates
08/21/17	Editorial updates in Figure 101 NVMe Management Interface Identify Controller from suggestions by Curtis Ballard and Michael Allison: a. Bits 7:2 – 1. Removed “decrement by one” 2. Adding initial count is “between 8 and 63” 3. Adding greater than “or equal” to 63 b. Bit 1 - Replacing “capable’ with “prohibited” c. Bit 0 - Adding “at time of manufacture”
08/21/17, pm	Editorial clarification on Vaux VPD write operation from Curtis Ballard: Replacing the “During the Auxiliary power, Vaux only, there shall be no VPD Write operation” with “During the Auxiliary power, Vaux only, if the Vaux VPD Write Prohibited bit in the Identify Controller data structure is set to one, then there shall be no VPD Write operation”.
08/22/17	Editorial updates in Figure 101, updating all Terms with Bold font
08/26/17	Clarifying on VPD Write Cycle Count bit 0 = 1 definition, suggestion from Michael Allison
09/13/17	Further clarifications from suggestions by Austin Bolen In Figure 101, adding Byte 253, Vaux Operation Prohibit Bits. Updated definitions for VPD Write Cycle and VPD Write Cycle Remaining Count in Byte 254
09/14/17	Further update from suggestion by Curtis and Austin, to make allow VPD write cycles with both 8 times and 100 times
09/21/17	Decided that there is no need to add the Vaux VPD Write Prohibited.
09/22/17	Updates from 9/22/17 conference call discussions.
09/24/17	Removed “multiple times”, make it to be same as before
09/25/17	More editorial changes from 9/25/17’s NVMe-MI call
10/02/17	One more editorial update from 9/25/17’s NVMe-MI call
1/28/18	Updated TP number to match NVMe numbering and TP administration contact info.

Description of Specification Change

Modify section 5.8 VPD Write:

The VPD Write command is used to update the Vital Product Data described in section 9.2.

The VPD Write command is used to update the Vital Product Data described in section 9.2er the VPD Write command completes successfully, reading the contents of the FRU Information Device directly or executing a VPD Read command shall return the new VPD contents (i.e., those supplied with the VPD Write command). The data to be written to the VPD is specified in the Request Data field. VPD Write uses NVMe Management Dwords 0 and 1 as shown in Figure 73 and Figure 74.

The VPD contents should be capable of being updated at least 8 ~~100~~ times using the VPD Write command (Editor Note, add this as a footnote: NVM Express Management Interface Specification, Revision 1.0a and prior recommended that VPD contents should be capable of being updated at least 100 times using the VPD Write command). If the initial value of the VPD Write Cycles Remaining field is less than 100, then the VPD Write Cycle Remaining Valid bit should be set to '1' (Refer to the VPD Information field in Figure 101). If there is an error preventing update of the VPD contents, then the Management Endpoint responds with a generic error response and VPD Writes Exceeded status.

Modify section 8.1 Identify Controller:

The NVMe Identify Controller data structure contains information about an NVMe Controller. Bytes 240-255 have been allocated by the NVM Express specification for NVMe-MI are defined below.

Figure 101: NVMe Management Interface Identify Controller

Bytes	O/M	Description
253:240		Reserved

<table>
<tr>
<td>254</td>
<td>M</td>
<td>VPD Write Cycle Information (VWCI): This field indicates information about remaining number of times that VPD contents are able to be updated using the VPD Write command.
<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>7</td><td>VPD Write Cycle Remaining Valid (VWCRV): If this bit is set to ‘1’ then the VPD Write Cycle Remaining field is valid. If this bit is cleared to ‘0’ then the VPD Write Cycles Remaining field is invalid and cleared to ‘0’.</td></tr>
<tr><td>6:0</td><td>VPD Write Cycles Remaining (VWCR): If the VPD Write Cycle Remaining Valid bit is set to ‘1’, then this field contains a value indicating the remaining number of times that VPD contents are able to be updated using the VPD Write command. If this field is set to 7Fh, then the remaining number of times that VPD contents are able to be updated using the VPD Write command is greater than or equal to 7Fh.

If the VPD Write Cycle Remaining Valid bit is cleared to ‘0’ then this field is not valid and shall be cleared to a value of 0h.</td></tr>
</table>
</td>
</tr>
<tr>
<td>255</td>
<td>M</td>
<td>Management Endpoint Capabilities (MEC): This field indicates the capabilities of the Management Endpoint in the Controller.

Bits 7:2 are reserved.

Bit 1: If set to ‘1’ then the NVM Subsystem contains a Management Endpoint on a PCIe port.

Bit 0: If set to ‘1’ then the NVM Subsystem contains a Management Endpoint on an SMBus/I2C port.</td>
</tr>
</table>