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NVM Express Technical Proposal for New Feature

Technical Proposal ID	**6006 – PCIe Port Numbering**
Change Date	**1/28/2018**
Builds on Specification	**NVM Express Management Interface 1.0a**

Technical Proposal Author(s)

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The NVMe-MI 1.0a specification requires that the Port Identifier for a PCIe port is the same as the Port Number field in the PCIe Link Capability Register. The effect of this requirement is that PCIe ports associated with NVM Subsystem need to have a unique PCIe port number. There is no requirement in the PCI Express Base Specification that ports associated with an Endpoint have unique port numbers. The purpose of this technical proposal is to remove the requirement that NVMe-MI imposes on PCIe.

Revision History

Revision Date	Change Description
10/9/2017	• Initial draft.
11/27/2017	• Updated text associated with Port Identifier field in the NVMe PCIe Port MultiRecord Area.
12/4/2017	• Fixed NVMe PCIe Port MultiRecord byte numbering.
1/28/2018	• Editorial changes to align with NVMe TP numbering, updated NVMe administration, and updated year.

Description of Specification Changes

Modify Section 1.4 as shown below:

1.4 Architectural Model

An NVMe storage device, such as a PCIe SSD, that implements this specification, consists of an NVM Subsystem with one or more Management Endpoints. There may be up to one Management Endpoint per PCIe port and SMBus/I2C port. Each Management Endpoint has a Port Identifier that is less than or equal to the Number of Ports (NUMP) field value in the NVM Subsystem Information Data Structure. ~~The Port Identifier for a PCIe port is the same as the Port Number field in the PCIe Link Capabilities Register.~~

NVMe-MI supports Vital Product Data (VPD) that utilizes the format defined in the IPMI Platform Management FRU Information Storage Definition and is stored in a FRU Information Device. The FRU Information Device may be implemented in the NVM Subsystem, in an external device (e.g., serial EEPROM), or a combination of the two. The VPD is accessible over any port that supports NVMe-MI using MCTP commands. If the NVMe storage device has an SMBus/I2C interface, then the VPD is accessible using the access mechanism over I2C as defined in the IPMI Platform Management FRU Information Storage Definition.

Modify Figure 64 as shown below:

Figure 64: PCIe Port Specific Data

<table>
<tr><th>Byte</th><th>Description</th></tr>
<tr><td>08</td><td>PCIe Maximum Payload Size: This field indicates the Max Payload Size for the specified PCIe port. If the link is not active, this field should be cleared to 0h.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>128 bytes</td></tr>
<tr><td>1h</td><td>256 bytes</td></tr>
<tr><td>2h</td><td>512 bytes</td></tr>
<tr><td>3h</td><td>1024 bytes</td></tr>
<tr><td>4h</td><td>2048 bytes</td></tr>
<tr><td>5h</td><td>4096 bytes</td></tr>
<tr><td>6h-FFh</td><td>Reserved</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>09</td><td>PCIe Supported Link Speeds Vector: This field indicates the Supported Link Speeds for the specified PCIe port.

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>7:3</td><td>Reserved</td></tr>
<tr><td>2</td><td>This bit shall be set to ‘1’ if the link supports 8.0 GT/s</td></tr>
<tr><td>1</td><td>This bit shall be set to ‘1’ if the link supports 5.0 GT/s</td></tr>
<tr><td>0</td><td>This bit shall be set to ‘1’ if the link supports 2.5 GT/s.</td></tr>
</table></td></tr>
<tr><td>10</td><td>PCIe Current Link Speed: The port’s PCIe negotiated link speed using the same encoding as the PCIe Supported Link Speed Vector field. A value of 0h in this field indicates the PCIe Link is not available.

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>Link not active</td></tr>
<tr><td>1h</td><td>The current link speed is the speed indicated in the supported link speed bit 0.</td></tr>
<tr><td>2h</td><td>The current link speed is the speed indicated in the supported link speed bit 1.</td></tr>
<tr><td>3h</td><td>The current link speed is the speed indicated in the supported link speed bit 2.</td></tr>
<tr><td>4h</td><td>The current link speed is the speed indicated in the supported link speed bit 3.</td></tr>
<tr><td>5h</td><td>The current link speed is the speed indicated in the supported link speed bit 4.</td></tr>
<tr><td>6h</td><td>The current link speed is the speed indicated in the supported link speed bit 5.</td></tr>
<tr><td>7h</td><td>The current link speed is the speed indicated in the supported link speed bit 6.</td></tr>
<tr><td>8h-FFh</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>11</td><td>PCIe Maximum Link Width: The maximum PCIe link width for this NVM Subsystem port. This is the expected negotiated link width that the port link trains to if the platform supports it. A Management Controller may compare this value with the PCIe Negotiated Link Width to determine if there has been a PCIe link training issue.

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>PCIe x1</td></tr>
<tr><td>2</td><td>PCIe x2</td></tr>
<tr><td>3</td><td>Reserved</td></tr>
<tr><td>4</td><td>PCIe x4</td></tr>
<tr><td>5-7</td><td>Reserved</td></tr>
<tr><td>8</td><td>PCIe x8</td></tr>
<tr><td>9-11</td><td>Reserved</td></tr>
<tr><td>12</td><td>PCIe x12</td></tr>
<tr><td>13-15</td><td>Reserved</td></tr>
<tr><td>16</td><td>PCIe x16</td></tr>
<tr><td>17-31</td><td>Reserved</td></tr>
<tr><td>32</td><td>PCIe x32</td></tr>
<tr><td>33-255</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>12</td><td>PCIe Negotiated Link Width: The negotiated PCIe link width for this port.

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0</td><td>Link not active</td></tr>
<tr><td>1</td><td>PCIe x1</td></tr>
<tr><td>2</td><td>PCIe x2</td></tr>
<tr><td>3</td><td>Reserved</td></tr>
<tr><td>4</td><td>PCIe x4</td></tr>
<tr><td>5-7</td><td>Reserved</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td></td><td><table>
<tr><td>8</td><td>PCIe x8</td></tr>
<tr><td>9-11</td><td>Reserved</td></tr>
<tr><td>12</td><td>PCIe x12</td></tr>
<tr><td>13-15</td><td>Reserved</td></tr>
<tr><td>16</td><td>PCIe x16</td></tr>
<tr><td>17-31</td><td>Reserved</td></tr>
<tr><td>32</td><td>PCIe x32</td></tr>
<tr><td>33-255</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>13</td><td>PCIe Port Number: This field contains the PCIe port number. This is the same value as that reported in the Port Number field in the PCIe Link Capabilities Register.</td></tr>
<tr><td>31:~~13~~14</td><td>Reserved</td></tr>
</table>

Modify Section 9.2.14 as shown below:

9.2.14 NVMe PCIe Port MultiRecord Area

Byte Offset	Factory Default	Description
00	0Ch	**NVMe PCIe Port Record Type ID**
01	2h	Bit 7 – end of list; record format version = 2h
02	28h	**Record Length (RLEN)**: This field indicates the length of the MultiRecord Area in bytes.
03	Impl Spec	**Record Checksum**: This field is used to give the record data a zero checksum (i.e., the modulo 256 sum of the record data bytes from byte offset 05 through the end of this record plus this checksum byte equals zero)
04	Impl Spec	**Header Checksum**: This field is used to give the record header a zero checksum (i.e., the modulo 256 sum of the preceding record bytes starting with the first byte of the header plus this checksum byte equals zero).
05	~~01~~h	**NVMe PCIe Port MultiRecord Area Version Number:** This field indicates the version number of this multirecord. This field shall be set to ~~zero~~ one in this version of the specification.
06	Impl Spec	**PCIe Port Number:** This field contains the PCIe port number. This is the same value as that reported in the Port Number field in the PCIe Link Capabilities Register.
07	Impl	**Port Information:** This field indicates information about the PCIe Ports in the device. Bits 7 to 1 are reserved. Bit 0, if set to '1' indicates that all PCIe ports within the device have the same capabilities (i.e., the capabilities listed in this structure are consistent across each PCIe port.
08	Impl Spec	**PCIe Link Speed:** This field indicates a bit vector of link speeds supported by the PCIe port. <table><tr><th>Bit</th><th>Definition</th></tr><tr><td>7:3</td><td>Reserved</td></tr><tr><td>2</td><td>Set to '1' if the PCIe link supports 8.0 GT/s. Otherwise cleared to '0'.</td></tr></table>

<table>
<tr><td></td><td></td><td><table>
<tr><td>1</td><td>Set to ‘1’ if the PCIe link supports 5.0 GT/s. Otherwise cleared to ‘0’.</td></tr>
<tr><td>0</td><td>Set to ‘1’ if the PCIe link supports 2.5 GT/s. Otherwise cleared to ‘0’.</td></tr>
</table></td></tr>
<tr><td>09</td><td>Impl Spec</td><td>PCIe Maximum Link Width: The maximum PCIe link width for this NVM Subsystem port. This is the expected negotiated link width that the port link trains to if the platform supports it. A Management Controller may compare this value with the PCIe Negotiated Link Width to determine if there has been a PCIe link training issue.

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>PCIe x1</td></tr>
<tr><td>2</td><td>PCIe x2</td></tr>
<tr><td>3</td><td>Reserved</td></tr>
<tr><td>4</td><td>PCIe x4</td></tr>
<tr><td>5-7</td><td>Reserved</td></tr>
<tr><td>8</td><td>PCIe x8</td></tr>
<tr><td>9-11</td><td>Reserved</td></tr>
<tr><td>12</td><td>PCIe x12</td></tr>
<tr><td>13-15</td><td>Reserved</td></tr>
<tr><td>16</td><td>PCIe x16</td></tr>
<tr><td>17-31</td><td>Reserved</td></tr>
<tr><td>32</td><td>PCIe x32</td></tr>
<tr><td>33-255</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>10</td><td>Impl Spec</td><td>MCTP Support: This field contains a bit vector that specifies the level of support for the NVMe Management Interface.

Bits 7 to 1 are reserved.

Bit 0, if set to ‘1’ indicates that MCTP based management commands are supported on the PCIe port.</td></tr>
<tr><td>11</td><td>Impl Spec</td><td>Ref Clk Capability: This field contains a bit vector that specifies the PCIe clocking modes supported by the port.

<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>7:4</td><td>Reserved</td></tr>
<tr><td>3</td><td>Set to ‘1’ if the device automatically uses RefClk if provided and otherwise uses SRIS. Otherwise cleared to ‘0’.</td></tr>
<tr><td>2</td><td>Set to ‘1’ if the PCIe link supports Separate ReClk with SSC (SRIS). Otherwise cleared to ‘0’.</td></tr>
<tr><td>1</td><td>Set to ‘1’ if the PCIe link supports Separate ReClk with no SSC (SRNS). Otherwise cleared to ‘0’.</td></tr>
<tr><td>0</td><td>Set to ‘1’ if the PCIe link supports common ReClk. Otherwise cleared to ‘0’.</td></tr>
</table></td></tr>
<tr><td>12</td><td>Impl Spec</td><td>Port Identifier: This field contains the NVMe-MI Port Identifier.</td></tr>
<tr><td>15:~~12~~ 13</td><td>00h</td><td>Reserved</td></tr>
</table>