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NVM Express Technical Proposal for New Feature

Technical Proposal ID	**6017 – VPD Data Structure Enhancement**
Change Date	**June 3, 2020**
Builds on Specification	**NVM Express Management Interface 1.1**

Technical Proposal Author(s)

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The purpose of this Technical Proposal is to eliminate unintended fixed sizes in the VPD for the NVMe MultiRecord Area and the NVMe PCIe Port MultiRecord Area. These records have a length field that was set to a fixed value which required a total of 30 bytes of padding. By changing the length value to implementation specific as prior changes for NVMe-MI 1.1 made to the Product Info Area we achieve consistency across all the MultiRecord length fields. This offers implementers the flexibility of eliminating the padding when VPD approaches 256 bytes. Thus extending the life of designs before requiring implementation of TP6013. This TP does not require the elimination of the padding for products that have sufficient space.

Revision History

Revision Date	Change Description
02/03/2020	First published draft
02/10/2020	Added feedback from workgroup to make padding optional instead of variable sized
03/23/2020.	Cleaned up text change to standard if-then syntax and put reserved back in
03/24/2020	Fixed date, updated values to use xxh for consistency. Accepted all changes.
6/2/2020	Integrated into the NVMe Management Interface Specification, Revision 1.1.
6/3/2020	Accepted all changes
6/3/2020	Added showing change from 00h to 0h in figure 149.

Description of Specification Changes

Editor's note: These changes are applied on top of NVMe-MI 1.1.

Modify Figure 148 NVMe MultiRecord Area as shown below:

<table>
<tr><th>Byte Offset</th><th>Factory Default</th><th>Description</th></tr>
<tr><td>00</td><td>0Bh</td><td>NVMe Record Type ID</td></tr>
<tr><td>01</td><td>02h or 82h</td><td>Record Format:
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>7</td><td>Set to '1' if last record in list.</td></tr>
<tr><td>6:0</td><td>Record format version = 2.</td></tr>
</table></td></tr>
<tr><td>02</td><td>20h or 3Bh</td><td>Record Length (RLEN): This field indicates the length of the MultiRecord Area in bytes without including the first 5 bytes that are common to all MultiRecords.</td></tr>
<tr><td>03</td><td>Impl Spec</td><td>Record Checksum: This field is used to give the record data a zero checksum (i.e., the modulo 256 sum of the record data bytes from byte offset 05 to the end of this record plus this checksum byte equals zero).</td></tr>
<tr><td>04</td><td>Impl Spec</td><td>Header Checksum: This field is used to give the record header a zero checksum (i.e., the modulo 256 sum of the first byte of the header through this checksum byte equals zero).</td></tr>
<tr><td>05</td><td>0h</td><td>NVMe MultiRecord Area Version Number: This field indicates the version number of this NVMe MultiRecord. This field shall be cleared to 0h in this version of the specification.</td></tr>
<tr><td>06</td><td>Impl Spec</td><td>Form Factor (FF): This field indicates the form factor of the Management Endpoint. Refer to the values in Figure 157.</td></tr>
<tr><td>12:07</td><td>0h</td><td>Reserved</td></tr>
<tr><td>13</td><td>Impl Spec [1]</td><td>Initial 1.8 V Power Supply Requirements: This field specifies the initial 1.8 V power supply requirements in Watts prior to receiving a Set Slot Power message.</td></tr>
<tr><td>14</td><td>Impl Spec [1]</td><td>Maximum 1.8 V Power Supply Requirements: This field specifies the maximum 1.8 V power supply requirements in Watts.</td></tr>
<tr><td>15</td><td>Impl Spec [1]</td><td>Initial 3.3 V Power Supply Requirements: This field specifies the initial 3.3 V power supply requirements in Watts prior to receiving a Set Slot Power message.</td></tr>
<tr><td>16</td><td>Impl Spec [1]</td><td>Maximum 3.3 V Power Supply Requirements: This field specifies the maximum 3.3 V power supply requirements in Watts.</td></tr>
<tr><td>17</td><td>0h</td><td>Reserved</td></tr>
<tr><td>18</td><td>Impl Spec [1]</td><td>Maximum 3.3 V aux Power Supply Requirements: This field specifies the maximum 3.3 V power supply requirements in 10 mW units.</td></tr>
<tr><td>19</td><td>Impl Spec [1]</td><td>Initial 5 V Power Supply Requirements: This field specifies the initial 5 V power supply requirements in Watts prior to receiving a Set Slot Power message.</td></tr>
<tr><td>20</td><td>Impl Spec [1]</td><td>Maximum 5 V Power Supply Requirements: This field specifies the maximum 5 V power supply requirements in Watts.</td></tr>
<tr><td>21</td><td>Impl Spec [1]</td><td>Initial 12 V Power Supply Requirements: This field specifies the initial 12 V power supply requirements in Watts prior to receiving a Set Slot Power message.</td></tr>
<tr><td>22</td><td>Impl Spec [1]</td><td>Maximum 12 V Power Supply Requirements: This field specifies the maximum 12 V power supply requirements in Watts.</td></tr>
<tr><td>23</td><td>Impl Spec</td><td>Maximum Thermal Load: This field specifies the maximum thermal load from the NVM Subsystem in Watts.</td></tr>
<tr><td>36:24</td><td>Impl Spec</td><td>Total NVM Capacity: This field indicates the total NVM capacity of the NVM Subsystem in bytes.</td></tr>
</table>

Byte Offset	Factory Default	Description
		If the NVM Subsystem supports Namespace Management, then this field should correspond to the value reported in the TNVMCAP field in the NVMe Identify Controller Data Structure. A value of 0h may be used to indicate this feature is not supported.
63:37	0h	~~Reserved~~ If the RLEN field is set to 3Bh, then this field is reserved. If the RLEN field is set to 20h, then this field is not present.
NOTES: 1. Power supply requirements shall be set to the smallest integer value which fully supplies the necessary power to the NVMe Storage Device. A value of 0h indicates that the power supply voltage is not used.		

Modify Figure 149 NVMe PCIe Port MultiRecord Area as shown below:

Byte Offset	Factory Default	Description
00	0Ch	**NVMe PCIe Port Record Type ID**
01	02h or 82h	**Record Format:** **Bit** / **Definition** 7 / Set to '1' if last record in list. 6:0 / Record format version = 2.
02	08h or 0Bh	**Record Length (RLEN):** This field indicates the length of the MultiRecord Area in bytes without including the first 5 bytes that are common to all MultiRecords.
03	Impl Spec	**Record Checksum:** This field is used to give the record data a zero checksum (i.e., the modulo 256 sum of the record data bytes from byte offset 05 to the end of this record plus this checksum byte equals zero).
04	Impl Spec	**Header Checksum:** This field is used to give the record header a zero checksum (i.e., the modulo 256 sum of the first byte of the header through this checksum byte equals zero).
05	1h	**NVMe PCIe Port MultiRecord Area Version Number:** This field indicates the version number of this NVMe PCIe Port MultiRecord. This field shall be set to 1h in this version of the specification.
06	Impl Spec	**PCIe Port Number:** This field contains the PCIe port number. This is the same value as that reported in the Port Number field in the PCIe Link Capabilities Register.
07	Impl Spec	**Port Information:** This field indicates information about the PCIe Ports in the device. Bits 7:1 are reserved. Bit 0, if set to '1' indicates that all PCIe ports within the device have the same capabilities (i.e., the capabilities listed in this structure are consistent across each PCIe port).
08	Impl Spec	**PCIe Link Speed:** This field indicates a bit vector of link speeds supported by the PCIe port. **Bit** / **Definition** 7:4 / Reserved 3 / Set to '1' if the PCIe link supports 16.0 GT/s, otherwise cleared to '0'. 2 / Set to '1' if the PCIe link supports 8.0 GT/s, otherwise cleared to '0'. 1 / Set to '1' if the PCIe link supports 5.0 GT/s, otherwise cleared to '0'. 0 / Set to '1' if the PCIe link supports 2.5 GT/s, otherwise cleared to '0'.

<table>
<tr><th>Byte Offset</th><th>Factory Default</th><th>Description</th></tr>
<tr><td>09</td><td>Impl Spec</td><td>PCIe Maximum Link Width: The maximum PCIe link width for this NVM Subsystem port. This is the expected negotiated link width that the port link trains to if the platform supports it. A Requester may compare this value with the PCIe Negotiated Link Width to determine if there has been a PCIe link training issue.

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>PCIe x1</td></tr>
<tr><td>2</td><td>PCIe x2</td></tr>
<tr><td>3</td><td>Reserved</td></tr>
<tr><td>4</td><td>PCIe x4</td></tr>
<tr><td>5 to 7</td><td>Reserved</td></tr>
<tr><td>8</td><td>PCIe x8</td></tr>
<tr><td>9 to 11</td><td>Reserved</td></tr>
<tr><td>12</td><td>PCIe x12</td></tr>
<tr><td>13 to 15</td><td>Reserved</td></tr>
<tr><td>16</td><td>PCIe x16</td></tr>
<tr><td>17 to 31</td><td>Reserved</td></tr>
<tr><td>32</td><td>PCIe x32</td></tr>
<tr><td>33 to 255</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>10</td><td>Impl Spec</td><td>MCTP Support: This field contains a bit vector that specifies the level of support for the NVMe Management Interface.

Bits 7:1 are reserved.
Bit 0, if set to ‘1’ indicates that MCTP-based management commands are supported on the PCIe port.</td></tr>
<tr><td>11</td><td>Impl Spec</td><td>Ref Clk Capability: This field contains a bit vector that specifies the PCIe clocking modes supported by the port.

<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>7:4</td><td>Reserved</td></tr>
<tr><td>3</td><td>Set to ‘1’ if the device automatically uses RefClk if provided and otherwise uses SRIS, otherwise cleared to ‘0’.</td></tr>
<tr><td>2</td><td>Set to ‘1’ if the PCIe link supports Separate RefClk with SSC (SRIS), otherwise cleared to ‘0’.</td></tr>
<tr><td>1</td><td>Set to ‘1’ if the PCIe link supports Separate RefClk with no SSC (SRNS), otherwise cleared to ‘0’.</td></tr>
<tr><td>0</td><td>Set to ‘1’ if the PCIe link supports common RefClk, otherwise cleared to ‘0’.</td></tr>
</table></td></tr>
<tr><td>12</td><td>Impl Spec</td><td>Port Identifier: This field contains the NVMe-MI Port Identifier.</td></tr>
<tr><td>15:13</td><td>~~0~~0h</td><td>~~Reserved~~
If the RLEN field is set to 0Bh, then this field is reserved. If the RLEN field is set to 08h, then this field is not present.</td></tr>
</table>