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Revision Date	**2024.04.26**
Builds on Specification(s)	**NVM Express Base Specification 2.0c**
References	

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Technical Proposal Overview

This proposal adds new host-initiated refresh operation as part of the Device Self-test command. The new operation provides a method for the host to inform the controller that it may perform internal refresh operation.

Revision History

Revision Date	Change Description
2023.02.20	Initial draft
2023.03.15	Incorporated Dan H. proposed changes.
2023.03.22	Incorporated additional changes.
2023.04.16	Added text for behavior on multiple controllers
2023.05.01	Minor editorial modifications
2023.09.07	Remove FigTBD (Format NVM command Aborting a Device Self-Test Operation) and some editorial modifications.
2023.09.13	Text clarification in section 8.6.TBD regarding the feature's scope and media extent as part of the operation
2023.09.28	More text clarification in section 8.6.TBD: Remove text regarding the Device Self-Test log page and status codes content
2023.10.09	Clean version to start Phase 3
2023.10.26	Text modification in section 8
2023.11.01	More editorial modifications: • Remove 'vendor specific' text • Setting the exact bits in the Current Device Self-test Status field in the Device Self-test log page • Adding a clear statement that the Host-Initiated Refresh operation is a device self-test operation
2023.11.09	Clean version for member review ballot
2024.03.25	Clean version for integration
2024.04.25	Integrated
2024.04.26	Fixed the Navigation pane nesting levels

Description for Changes Document for NVM Express Base Specification 2.0

New Features/Feature Enhancements/Required Changes:

- Host Initiated Refresh operation (optional)
    - Description of change.
        - Optional new operation as part of the DST command
        - Update the Device Self-test Log page
    - **New requirement and incompatible change**
        - none
    - References
        - Technical Proposal TP4058

Markup Conventions:

Black:	Unchanged (however, hot links are removed)
~~Red Strikethrough~~:	Deleted
Blue:	New
Blue Highlighted:	TBD values, anchors, and links to be inserted in new text.
<Green Bracketed>:	Notes to editor

Description of Specification Changes for the NVM Express Base Specification 2.0c

Modify portions of section 5 as shown below:

5 Admin Command Set

5.9 Device Self-test command

The Device Self-test command is used to start a device self-test operation or abort a device self-test operation (refer to section 8.8). The Device Self-test command is used specifically to:

a) start a short device self-test operation;
b) start an extended device self-test operation;
c) start a Host-Initiated Refresh operation;
d) start a vendor specific device self-test operation; or
e) abort a device self-test operation already in process.

A Host-Initiated Refresh operation is a device self-test operation.

The device self-test operation is performed by the controller that the Device Self-test command was submitted to. The Namespace Identifier field controls which namespaces are included in the device self-test operation as specified in Figure 177. For a Host-Initiated Refresh operation, the Namespace Identifier field shall be ignored by the controller.

Figure 177: Device Self-test Namespace Test Action

NSID Value	Description
00000000h	Specifies that the device self-test operation shall not include any namespaces, and only the controller is included as part of the device self-test operation.
00000001h to FFFFFFFEh	Specifies that the device self-test operation shall include the namespace specified by this field. If this field specifies an invalid namespace ID, then the controller shall abort the command with a status code of Invalid Namespace or Format. If this field specifies an inactive namespace ID, then the controller shall abort the command with a status code of Invalid Field in Command.
FFFFFFFFh	Specifies that the device self-test operation shall include all active namespaces accessible through the controller at the time the device self-test operation is started.

The Device Self-test command uses the Command Dword 10 field and the Command Dword 15 field. All other command specific fields are reserved.

Figure 178: Device Self-test – Command Dword 10

Bits	Description
31:04	Reserved

Figure 178: Device Self-test – Command Dword 10

Bits	Description
03:00	**Self-test Code (STC):** This field specifies the action taken by the Device Self-test command. **Value** / **Definition** 0h / Reserved 1h / Start a short device self-test operation 2h / Start an extended device self-test operation 3h / Start a Host-Initiated Refresh operation ~~3h~~4h to Dh / Reserved Eh / Vendor specific. Additional information may be provided in Command Dword 15 (refer to Figure 179). Fh / Abort device self-test operation

Figure 179: Device Self-test – Command Dword 15

Bits	Description
31:00	If the Self-test Code field is set to Eh (refer to Figure 178), then this field is vendor specific; otherwise this field is reserved.

The processing of a Device Self-test command and interactions with a device self-test operation already in progress is defined in Figure 180.

Figure 180: Device Self-test – Command Processing

Self-test in Progress [1]	Self-test Code value in new Drive Self-test command	Controller Action
Yes	1h – Short device self-test	Abort the new Device Self-test command with a status code of Device Self-test in Progress.
	2h – Extended device self-test	
	3h – Host-Initiated Refresh	
	Eh – Vendor specific	Vendor specific
	Fh – Abort device self-test	The controller takes the following actions in order: 1. Abort device self-test operation in progress; 2. Create log entry in the Newest Self-test Result Data Structure in the Device Self-test Log; 3. Set bits 3:0 of the Current Device Self-test Status field in the Device Self-test log page to 0h; and 4. Completes command successfully.
No	1h – Short device self-test	The controller takes the following actions in order: 1. Validate the command parameters; 2. Set bits 3:0 of the Current Device Self-test Status field in the Device Self-test log page to 1h; 3. Start a device self-test operation; and 4. Completes command successfully.
	2h – Extended device self-test	The controller takes the following actions in order: 1. Validate the command parameters; 2. Set bits 3:0 of the Current Device Self-test Status field in the Device Self-test log page to 2h; 3. Start a device self-test operation; and 4. Completes command successfully.
	3h – Host-Initiated Refresh	The controller takes the following actions in order: 1. Validate the command parameters; 2. Set bits 3:0 of the Current Device Self-test Status field in the Device Self-test log page to 3h; 3. Start a Host-Initiated Refresh operation; and 4. Complete the command successfully.
	Eh – Vendor specific	Vendor specific
	Fh – Abort device self-test	Completes command successfully. The Device Self-test Log is not modified.

Notes:
1. If bit 0 is cleared to '0' in the Device Self-test Options (DSTO) of the Identify Controller data structure (refer to Figure 307), then the Self-test in Progress column represents that a device self-test operation is in progress on the controller that the new Device Self-test command was received on. If bit 0 is set to '1' in the Device Self-test Options (DSTO) of the Identify Controller data structure, then the Self-test in Progress column represents that a device self-test operation is in progress on the NVM subsystem.

5.16 Get Log Page command

5.16.1 Log Specific Information

5.16.1.7 Device Self-test (Log Identifier 06h)

This log page is used to indicate:

a) the status of any device self-test operation in progress and the percentage complete of that operation; and

b) the results of the last 20 device self-test operations.

The Self-test Result Data Structure contained in the Newest Self-test Result Data Structure field is always the result of the last completed or aborted self-test operation. The next Self-test Result Data Structure field in the Device Self-test log page contains the results of the second newest self-test operation and so on. If fewer than 20 self-test operations have completed or been aborted, then the Device Self-test Status field shall be set to Fh in the unused Self-test Result Data Structure fields and all other fields in that Self-test Result Data Structure are ignored.

Figure 232: Device Self-test Log Page

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>00</td><td>Current Device Self-Test Operation: This field defines the current device self-test operation.

Bits 7:4 are reserved.

Bits 3:0 indicates the status of the current device self-test operation as defined in the following table. If a device self-test operation is in process (i.e., this field is set to 1h or 2h), then the controller shall not set this field to 0h until a new Self-test Result Data Structure is created (i.e., if a device self-test operation completes or is aborted, then the controller shall create a Self-test Result Data Structure prior to setting this field to 0h).
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>No device self-test operation in progress</td></tr>
<tr><td>1h</td><td>Short device self-test operation in progress</td></tr>
<tr><td>2h</td><td>Extended device self-test operation in progress</td></tr>
<tr><td>3h</td><td>Host-Initiated Refresh operation in progress</td></tr>
<tr><td>~~3h~~4h to Dh</td><td>Reserved</td></tr>
<tr><td>Eh</td><td>Vendor specific</td></tr>
<tr><td>Fh</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>01</td><td>Current Device Self-Test Completion: This field defines the completion status of the current device self-test.

Bit 7 is reserved.

Bits 6:0 indicates the percentage of the device self-test operation that is complete (e.g., a value of 25 indicates that 25% of the device self-test operation is complete and 75% remains to be tested). If bits 3:0 in the Current Device Self-Test Operation field are cleared to 0h (indicating there is no device self-test operation in progress), then this field is ignored.</td></tr>
<tr><td>03:02</td><td>Reserved</td></tr>
<tr><td>31:04</td><td>Newest Self-test Result Data Structure (refer to Figure 233)</td></tr>
<tr><td>59:32</td><td>2nd newest Self-test Result Data Structure (refer to Figure 233)</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>535:508</td><td>19th newest Self-test Result Data Structure (refer to Figure 233)</td></tr>
<tr><td>563:536</td><td>20th newest Self-test Result Data Structure (refer to Figure 233)</td></tr>
</table>

Figure 233: Self-test Result Data Structure

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>00</td><td>
Device Self-test Status: This field indicates the device self-test code and the status of the operation.

Bits 7:4 indicates the Self-test Code value that was specified in the Device Self-test command that started the device self-test operation that this Self-test Result Data Structure describes.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>Reserved</td></tr>
<tr><td>1h</td><td>Short device self-test operation</td></tr>
<tr><td>2h</td><td>Extended device self-test operation</td></tr>
<tr><td>3h</td><td>Host-Initiated Refresh operation</td></tr>
<tr><td>~~3h~~4h to Dh</td><td>Reserved</td></tr>
<tr><td>Eh</td><td>Vendor specific</td></tr>
<tr><td>Fh</td><td>Reserved</td></tr>
</table>
Bits 3:0 indicates the result of the device self-test operation that this Self-test Result Data Structure describes.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>Operation completed without error</td></tr>
<tr><td>1h</td><td>Operation was aborted by a Device Self-test command</td></tr>
<tr><td>2h</td><td>Operation was aborted by a Controller Level Reset</td></tr>
<tr><td>3h</td><td>Operation was aborted due to a removal of a namespace from the namespace inventory</td></tr>
<tr><td>4h</td><td>Operation was aborted due to the processing of a Format NVM command</td></tr>
<tr><td>5h</td><td>A fatal error or unknown test error occurred while the controller was executing the device self-test operation and the operation did not complete</td></tr>
<tr><td>6h</td><td>Operation completed with a segment that failed and the segment that failed is not known</td></tr>
<tr><td>7h</td><td>Operation completed with one or more failed segments and the first segment that failed is indicated in the Segment Number field</td></tr>
<tr><td>8h</td><td>Operation was aborted for unknown reason</td></tr>
<tr><td>9h</td><td>Operation was aborted due to a sanitize operation</td></tr>
<tr><td>Ah to Eh</td><td>Reserved</td></tr>
<tr><td>Fh</td><td>Entry not used (does not contain a test result)</td></tr>
</table>
</td></tr>
<tr><td>01</td><td>Segment Number: This field indicates the segment number (refer to section 8.8) where the first self-test failure occurred. If Device Self-test Status field bits [3:0] are not set to 7h, then this field should be ignored.</td></tr>
<tr><td>02</td><td>
Valid Diagnostic Information: This field indicates the diagnostic failure information that is reported.

Bits 7:4 are reserved.

Bit 3 (SC Valid): If set to ‘1’, then the contents of Status Code field are valid. If cleared to ‘0’, then the contents of the Status Code field are invalid.

Bit 2 (SCT Valid): If set to ‘1’, then the contents of the Status Code Type field are valid. If cleared to ‘0’, then the contents of the Status Code Type field are invalid.

Bit 1 (FLBA Valid): If set to ‘1’, then the contents of the Failing LBA field are valid. If cleared to ‘0’, then the contents of the Failing LBA field are invalid.

Bit 0 (NSID Valid): If set to ‘1’, then the contents of the Namespace Identifier field are valid. If cleared to ‘0’, then the contents of the Namespace Identifier field are invalid.
</td></tr>
<tr><td>03</td><td>Reserved</td></tr>
<tr><td>11:04</td><td>Power On Hours (POH): This field indicates the number of power-on hours at the time the device self-test operation was completed or aborted. This does not include time that the controller was powered and in a low power state condition.</td></tr>
</table>

Figure 233: Self-test Result Data Structure

Bytes	Description
15:12	**Namespace Identifier (NSID):** This field indicates the namespace that the Failing LBA occurred on. The contents of this field are valid only when the NSID Valid bit is set to '1'.
23:16	**Failing LBA:** This field is I/O Command Set specific and is described in the applicable I/O Command Set specification. NOTE: The original field name has been retained for historical continuity.
24	**Status Code Type:** This field may contain additional information related to errors or conditions. Bits 7:3 are reserved. Bits 2:0 may contain additional information relating to errors or conditions that occurred during the device self-test operation represented in the same format used in the Status Code Type field of the completion queue entry (refer to Figure 89). The contents of this field are valid only when the SCT Valid bit is set to '1'.
25	**Status Code:** This field may contain additional information relating to errors or conditions that occurred during the device self-test operation represented in the same format used in the Status Code field of the completion queue entry (refer to section 3.3.3.2.1). The contents of this field are valid only when the SC Valid bit is set to '1'.
27:26	Vendor Specific

5.17 Identify command...

5.17.2 Identify Data Structures

5.17.2.1 Identify Controller Data Structure (CNS 01h)

…

Figure 275: Identify – Identify Controller Data Structure, I/O Command Set Independent

Bytes	I/O[1]	Admin[1]	Disc[1]	Description
Controller Capabilities and Features				
…				
Admin Command Set Attributes & Optional Controller Capabilities				
…				
318	O	O	R	**Device Self-test Options (DSTO)**: This field indicates the optional Device Self-test command or operation behaviors supported by the controller or NVM subsystem. Bits 7:2~~1~~ are reserved. Bit 1 (**Host-Initiated Refresh Support (HIRS))** if set to '1', then the controller supports the Host-Initiated Refresh capability (refer to section 8.6.TBD). If cleared to '0', then the controller does not support the Host-Initiated Refresh capability. This bit shall be cleared to '0' if the controller does not support the Device Self-test command (i.e., bit 4 in the OACS field is cleared to '0'). If the controller does not support the Device Self-test command (i.e., bit 4 in the OACS field is cleared to '0'), then This bit shall be cleared to '0. Bit 0 if set to '1', then the NVM subsystem supports only one device self-test operation in progress at a time. If cleared to '0', then the NVM subsystem supports one device self-test operation per controller at a time.
…				
559:544	O	R	R	**Maximum Domain Namespace Attachments (MAXDNA):** Indicates the maximum of the sum of the number of namespaces attached to each I/O controller in the Domain. If this field is cleared to 0h, then no maximum is specified. The value of this field shall be the same value for all I/O controllers in the Domain.

Bytes	I/O[1]	Admin[1]	Disc[1]	Description
563:560	O	R	R	**Maximum I/O Controller Namespace Attachments (MAXCNA):** Indicates the maximum number of namespaces that are allowed to be attached to this I/O controller. If this field is cleared to 0h, then no maximum is specified. The value of this field shall be less than or equal to the number of namespaces supported by the NVM subsystem (refer to the MNAN field).
568	O	R	R	**Recommended Host-Initiated Refresh Interval (RHIRI)**: If the Host-Initiated Refresh capability is supported (i.e., the HIRS bit in the DSTO field is set to '1'), then this field indicates the recommended time interval in days from last power down to the time at which the host should initiate the Host-Initiated Refresh operation. If this field is cleared to 0h, then this field is not reported. If the HIRS bit in the DSTO field is cleared to '0', then This field shall be cleared to 0h.
569	O	R	R	**Host-Initiated Refresh Time (HIRT):** If the Host-Initiated Refresh capability is supported (i.e., the HIRS bit in the DSTO field is set to '1'), then this field indicates the nominal amount of time in minutes that the controller takes to complete the Host-Initiated Refresh operation. If this field is cleared to 0h, then this field is not reported. If the HIRS bit in the DSTO field is cleared to '0', then This field shall be cleared to 0h.
767:~~564~~ 570				Reserved
1023:768	M	M	R	**NVM Subsystem NVMe Qualified Name (SUBNQN):** This field specifies the NVM Subsystem NVMe Qualified Name as a UTF-8 null-terminated string. Refer to section 4.5 for the definition of NVMe Qualified Name. Support for this field is mandatory if the controller supports revision 1.2.1 or later as indicated in the Version property (refer to section 3.1.3.2).
…				

Modify portions of section 8 as shown below:

8 Extended Capabilities

8.6 Device Self-test Operations

A device self-test operation is a diagnostic testing sequence that tests the integrity and functionality of the controller and may include testing of the media associated with namespaces or refresh operations. The operation is broken down into a series of segments, where each segment is a set of vendor specific tests or refresh operations. The segment number in the Self-test Result Data Structure (refer to section 5.22.1.7) is used for reporting purposes to indicate where a test failed, if any. The test performed in each segment may be the same for the short device self-test operation and the extended device self-test operation.

A device self-test operation is performed in the background allowing concurrent processing of some commands and requiring suspension of the device self-test operation to process other commands. Which commands may be processed concurrently versus require suspension of the device self-test operation is vendor specific.

If the controller receives any command that requires suspension of the device self-test operation to process and complete, then the controller shall:

1) suspend the device self-test operation;
2) process and complete that command; and

3) resume the device self-test operation.

During a device self-test operation, the performance of the NVM subsystem may be degraded (e.g., controllers not performing the device self-test operation may also experience degraded performance).

The following device self-test operations are defined:

a) short device self-test operation (refer to section 8.6.1); ~~and~~
b) extended device self-test operation (refer to section 8.6.2)~~.~~; and
c) Host-Initiated Refresh operation (refer to section 8.6.TBD).

Figure 570 is an informative example of a device self-test operation with the associated segments and tests performed in each segment.

Figure 570: Example Device Self-test Operation (Informative)

Segment		Test Performed	Failure Criteria
1 – RAM Check		Write a test pattern to RAM, followed by a read and compare of the original data.	Any uncorrectable error or data miscompare
2 – SMART Check		Check SMART or health status for Critical Warning bits set to '1' in SMART / Health Information Log.	Any Critical Warning bit set to '1' fails this segment
3 – Volatile memory backup		Validate volatile memory backup solution health (e.g., measure backup power source charge and/or discharge time).	Significant degradation in backup capability
4 – Metadata validation		Confirm/validate all copies of metadata.	Metadata is corrupt and is not recoverable
5 – NVM integrity		Write/read/compare to reserved areas of each NVM. Ensure also that every read/write channel of the controller is exercised.	Data miscompare
Extended only	6 – Data Integrity	Perform background housekeeping tasks, prioritizing actions that enhance the integrity of stored data. Exit this segment in time to complete the remaining segments and meet the timing requirements for extended device self-test operation indicated in the Identify Controller data structure.	Metadata is corrupt and is not recoverable
7 – Media Check		Perform random reads from every available good physical block. Exit this segment in time to complete the remaining segments. The time to complete is dependent on the type of device self-test operation.	Inability to access a physical block
8 – Drive Life		End-of-life condition: Assess the drive's suitability for continuing write operations.	The Percentage Used is set to 255 in the SMART / Health Information Log or an analysis of internal key operating parameters indicates that data is at risk if writing continues
9 – SMART Check		Same as 2 – SMART Check	

8.6.TBD Host-Initiated Refresh Operation

The Host-Initiated Refresh operation of the Device Self-test command performs implementation-specific refresh operations that verify the media integrity and ensure access to media (e.g., media in an NVM subsystem that has not been in operation for a long period of time and/or has been subject to extreme environmental conditions). Examples of refresh operations may include read verification, rewrite of underlying media that are exhibiting a high correctable error rate (e.g., to prevent future errors), and other maintenance activities. A Host-Initiated Refresh operation does not change stored user data.

If the Host-Initiated Refresh operation is supported, then the controller shall set the HIRS bit to ‘1’ in the DSTO field in the Identify Controller data structure (refer to Figure 275).

The percentage complete of the Host-Initiated Refresh operation is indicated in the Current Percentage Complete field in the Device Self-test log page (refer to section 5.16.1.7).

For Host-Initiated Refresh operation, the NSID field in the Device Self-test command is ignored by the controller and all media in the NVM subsystem is refreshed regardless of whether any portion of the media is or is not part of any namespace.

A Host-Initiated Refresh operation shall be aborted:

a) if any Controller Level Reset affects the controller on which the device self-test is being performed;
b) if a Format NVM command is processed by any controller in the NVM subsystem;
c) if a sanitize operation is started (refer to section 5.24); or
d) if a Device Self-test command with the Self-Test Code field set to Fh is processed by any controller in the NVM subsystem.

A Controller Level Reset on a controller that is not performing the Host-Initiated Refresh operation shall not impact that Host-Initiated Refresh operation.