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NVM Express Workgroup
c/o VTM Group
3855 SW 153rd Drive
Beaverton, OR 97003 USA
info@nvmexpress.org

NVM Express Technical Proposal for New Feature

Technical Proposal ID	**4051**
Change Date	**2019-02-19**
Builds on Specification(s)	**NVM Express 1.3c**
Referenced Ratified Technical Proposal(s)	**TP 4000a Persistent Memory Region**

Technical Proposal Author(s)

Name	**Company**
Mike Allison, Jonathan Hughes, Raymond Robles	Intel
Peter Onufryk	Microsemi
Judy Brock	Samsung

This technical proposal relaxes restrictions on the host usage of the Controller Buffer Memory.

Revision History

Revision Date	**Change Description**
2018-07-23	Initial version
2018-07-31	Moved new options to CMBLOC register; expanded initial 3 options to 5 options, renaming/word-smithing of new register bits
2018-08-01	Corrected the CBM queue requirement about a queue solely being contained in the CMB.
2018-08-14	Remove the usage of the word employed. Fixed spelling.
2018-08-24	Fixed figures numbers to match NVMe 1.3c. Added I/O Submission Queues and I/O Completion Queues to be dword aligned if located in the Controller Memory Buffer,
2018-11-06	Fixing the functional change made by changing “may only” to “shall” in the changes for CMBLOC.CDPCILS bit as identified by Judy Brock.
2018-11-07	Updating the definition of CDPCILS based on the change from 2018-11-07.
2018-11-08	Wordsmithing the definition of CDPCILS. Corrected the definition of CDPMLS that was accidently changed with a cut/paste issue.
2018-12-05	More wordsmithing on text associated with CDPCILS
2019-01-15	30 member editorial changes and account for 2019.
2019-01-16	Editorial changes per member review comment: make PRP List and SGL be entirely in CMB or entirely outside CMB; make data and metadata be entirely in CMB or entirely outside CMB.
2019-01-17	Integration
2019-02-19	Ratified

Description for NVMe Changes Document

- The restrictions on the Controller Memory Buffer in relation to Submission queues, commands, and separation of data and metadata changed to use supported bits in the Controller Memory Buffer Size register. The Controller Memory Buffer section (refer to section 4.7) is modified to apply the

restrictions only if the newly added supported bits indicate the restrictions are enforced. All changes are backwards compatible.

Description of Specification Changes

The Controller Memory Buffer Size register added bits to control the Controller Memory Buffer restrictions to the Submission Queue, commands, and separation of data and metadata.

Markup Conventions:

Black:	Unchanged (however, hot links are removed)
~~Red Strikethrough~~:	Deleted
Red:	New
Red Highlighted:	TBD values, anchors, and links to be inserted.
<Green Bracketed>:	Notes to editor

Modify portions of section figure 3.1.11 (Offset 38h: CMBLOC – Controller Memory Buffer Location) as shown below:

Bits	Type	Reset	Description
31:12	RO	Impl Spec	**Offset (OFST):** Indicates the offset of the Controller Memory Buffer in multiples of the Size Unit specified in CMBSZ. This value shall be 4KB aligned.

Bits	Type	Reset	Description
11:~~03~~09	RO	0h	Reserved
08	RO	Impl Spec	**CMB Queue Dword Alignment (CQDA):** If this bit is set to '1', then I/O Submission Queues and I/O Completion Queues contained in the Controller Memory Buffer are dword aligned. If this bit is cleared to '0', then the I/O Submission Queues and I/O Completion Queues contained in the Controller Memory Buffer are aligned as defined by the PRP1 field of a Create I/O Submission Queue command (refer to Figure 55) or a Create I/O Completion Queue command (refer to Figure 51).
07	RO	Impl Spec	**CMB Data Metadata Mixed Memory Support (CDMMMS):** If this bit is set to '1', then the restriction on data and metadata use of Controller Buffer Memory by a command as defined in section 4.7 is not enforced. If this bit is cleared to '0', then the restriction on data and metadata use of Controller Buffer Memory by a command as defined in section 4.7 is enforced.
06	RO	Impl Spec	**CMB Data Pointer and Command Independent Locations Support (CDPCILS):** If this bit is set to '1', then the restriction that the PRP Lists and SGLs shall not be located in the Controller Buffer Memory if the command that they are associated with is not located in the Controller Buffer Memory is not enforced (refer to section 4.7). If this bit is cleared to '0', then that restriction is enforced.
05	RO	Impl Spec	**CMB Data Pointer Mixed Locations Support (CDPMLS):** If this bit is set to '1', then the restriction that for a particular PRP List or SGL associated with a single command, all memory that is associated with that particular PRP List or SGL shall reside in either the Controller Memory Buffer or outside the Controller Memory Buffer , is not enforced (refer to section 4.7). If this bit is cleared to '0', then that restriction is enforced.
04	RO	Impl Spec	**CMB Queue Physically Discontiguous Support (CQPDS):** If this bit is set to '1', then the restriction that for all queues in the Controller Memory Buffer, the queue shall be physically contiguous, is not enforced (refer to section 4.7). If this bit is cleared to '0', then that restriction is enforced.
03	RO	Impl Spec	**CMB Queue Mixed Memory Support (CQMMS):** If this bit is set to '1', then for a particular queue placed in the Controller Memory Buffer, the restriction that all memory associated with that queue shall reside in the Controller Memory Buffer is not enforced (refer to section 4.7). If this bit is cleared to '0', then that requirement is enforced.
02:00	RO	Impl Spec	**Base Indicator Register (BIR):** Indicates the Base Address Register (BAR) that contains the Controller Memory Buffer. For a 64-bit BAR, the BAR for the lower 32-bits of the address is specified. Values 0h, 2h, 3h, 4h, and 5h are valid.

Modify portions of section 4.7 (Controller Memory Buffer) as shown below:

A controller memory based queue is used in the same manner as a host memory based queue – the difference is the memory address used is located within the controller's own memory rather than in the host memory. The Admin or I/O Queues may be placed in the Controller Memory Buffer. If the CMBLOC.CQMMS bit (refer to Figure 82) is cleared to '0', then for ~~For~~ a particular queue, all memory associated with it shall reside in either the Controller Memory Buffer or ~~host memory~~ outside the Controller Memory Buffer.

If the CMBLOC.CQPDS bit (refer to Figure 82) is cleared to '0', then for ~~For~~ all queues in the Controller Memory Buffer, the queue shall be physically contiguous.

The controller may support PRP Lists and SGLs in the Controller Memory Buffer. If the CMBLOC.CDPMLS bit (refer to Figure 82) is cleared to '0', then for ~~For~~ a particular PRP List or SGL associated with a single command, all memory associated with the PRP List or SGL~~s~~ shall be ~~reside in~~ either entirely located in the Controller Memory Buffer or ~~host memory~~ entirely located outside the Controller Memory Buffer.

~~The~~ PRP Lists and SGLs associated with~~for~~ a command may ~~only~~ be placed in the Controller Memory Buffer if ~~the associated~~ that command is present in a Submission Queue in the Controller Memory Buffer. If:

a) CMBLOC.CDPCILS bit (refer to Figure 82) is cleared to '0'; and
b) a command is not present in a Submission Queue in the Controller Memory Buffer,

then the PRP Lists and SGLs associated with that command shall not be placed in the Controller Memory Buffer.

The controller may support data and metadata in the Controller Memory Buffer. If the CMBLOC.CDMMMS bit (refer to Figure 82) is cleared to '0', then ~~A~~all data and metadata, if any, associated with a particular command shall be either entirely located in the Controller Memory Buffer or entirely located outside the Controller Memory Buffer.

If the requirements for the Controller Memory Buffer use are violated by the host, the controller shall fail the associated command with Invalid Use of Controller Memory Buffer status.

Modify portions of figure 51 (Create I/O Completion Queue – PRP Entry 1) as shown below:

63:00	**PRP Entry 1 (PRP1):** If CDW11.PC is set to '1', then this field specifies a 64-bit base memory address pointer of the Completion Queue that is physically contiguous ~~and~~. The address pointer is memory page aligned (based on the value in CC.MPS) unless otherwise specified. If CDW11.PC is cleared to '0', then this field specifies a PRP List pointer that describes the list of pages that constitute the Completion Queue ~~and~~. The list of pages is memory page aligned (based on the value in CC.MPS) unless otherwise specified. In both cases the PRP Entry shall have an offset of 0h. In a non-contiguous Completion Queue, each PRP Entry in the PRP List shall have an offset of 0h. If there is a PRP Entry with a non-zero offset, then the controller should return an error of PRP Offset Invalid.

Modify a portion of figure 53 (Create I/O Completion Queue – Command Dword 11) as shown below:

00	**Physically Contiguous (PC):** If set to '1', then the Completion Queue is physically contiguous and PRP Entry 1 (PRP1) is the address of a contiguous physical buffer. If cleared to '0', then the Completion Queue is not physically contiguous and PRP Entry 1 (PRP1) is a PRP List pointer. If the: • queue is located in the Controller Memory Buffer; • ~~and~~ PC is cleared to '0'~~,~~; and • CMBLOC.CQPDS is cleared to '0', then the controller shall fail the command with Invalid Use of Controller Memory Buffer status.

Modify portions of figure 55 (Create I/O Submission Queue – PRP Entry 1) as shown below:

63:00	**PRP Entry 1 (PRP1):** If CDW11.PC is set to '1', then this field specifies a 64-bit base memory address pointer of the Submission Queue that is physically contiguous ~~and~~. The address pointer is memory page aligned (based on the value in CC.MPS) unless otherwise specified. If CDW11.PC is cleared to '0', then this field specifies a PRP List pointer that describes the list of pages that constitute the Submission Queue ~~and~~. The list of pages is memory page aligned (based on the value in CC.MPS) unless otherwise specified. In both cases, the PRP Entry shall have an offset of 0h. In a non-contiguous Submission Queue, each PRP Entry in the PRP List shall have an offset of 0h. If there is a PRP Entry with a non-zero offset, then the controller should return an error of PRP Offset Invalid.

Modify a portion of figure 57 (Create I/O Submission Queue – Command Dword 11) as shown below:

00	**Physically Contiguous (PC):** If set to '1', then the Submission Queue is physically contiguous and PRP Entry 1 (PRP1) is the address of a contiguous physical buffer. If cleared to '0', then the Submission Queue is not physically contiguous and PRP Entry 1 (PRP1) is a PRP List pointer. If this bit is cleared to '0' and CAP.CQR is set to '1', the controller should return an error of Invalid Field in Command. If the: • queue is located in the Controller Memory Buffer; • ~~and~~ PC is cleared to '0'~~,~~; and • CMBLOC.CQPDS is cleared to '0', then the controller shall fail the command with Invalid Use of Controller Memory Buffer status.